WHAT IS CLAIMED IS:

1. A multi-chip package device comprising:

a plurality of package terminals;

a semiconductor memory chip having a test circuit and a test terminal, the test circuit is enabled when a high voltage level is applied to the test terminal; and

an interface chip connected to the package terminals and the semiconductor memory, the interface chip including,

a control circuit having a plurality of memory terminals connected to the package terminals, the control circuit generating a test signal and an enable signal in response to signals received from the memory terminals,

a high voltage generating circuit connected to the control circuit, the high voltage generating circuit generates a high voltage signal having the high voltage level in response to the enable signal, and

a transferring circuit connected to the control circuit, the high voltage circuit and the test terminal of the memory chip, the transferring circuit providing the high voltage signal to the memory chip in response to the test signal.

2. A multi-chip package device according to claim 1, wherein the memory terminals are serial interface memory terminals.

3. A multi-chip package device according to claim

2, wherein the serial interface memory terminals includes a chip select terminals, a serial data input terminal, a serial data output terminal and a clock input terminal.

4. A multi-chip package device according to claim 1, wherein the memory chip is a general purpose memory chip.

5. A multi-chip package device according to claim 1, wherein the transferring circuit includes a P channel MOS transistor having a gate connected to receive the test signal, a first terminal connected to receive the high voltage signal and a second terminal connected to the test terminal.

6. A multi-chip package device according to claim 1, wherein the control circuit receives the high voltage signal, and wherein the test signal has the high voltage level.

7. A multi-chip package device comprising:

a plurality of package terminals;

a semiconductor memory chip having a test circuit, a plurality of address input terminals and a test terminal, the test circuit is enabled when a high voltage level is applied to the test terminal; and

an interface chip connected to the package terminals and the semiconductor memory, the interface chip including,

a control circuit having a plurality of memory terminals connected to the package terminals and a

plurality of address terminals for providing address signals based on signals received from the memory terminals, the control circuit generating a test signal and an enable signal in response to the received signals,

a high voltage generating circuit connected to the control circuit, the high voltage generating circuit generates a high voltage signal having the high voltage level in response to the enable signal, and

a transferring circuit connected to the control circuit, the high voltage circuit and the test terminal of the memory chip, the transferring circuit providing the high voltage signal to the memory chip in response to the test signal.

8. A multi-chip package device according to claim 7, wherein the memory terminals are serial interface memory terminals.

9. A multi-chip package device according to claim 8, wherein the serial interface memory terminals includes a chip select terminals, a serial data input terminal, a serial data output terminal and a clock input terminal.

10. A multi-chip package device according to claim 7, wherein the memory chip is a general purpose memory chip.

11. A multi-chip package device according to claim 7, wherein the transferring circuit includes a P channel MOS transistor having a gate connected to receive the test signal, a first terminal connected to receive the

high voltage signal and a second terminal connected to the test terminal.

12. A multi-chip package device according to claim 7, wherein the control circuit receives the high voltage signal, and wherein the test signal has the high voltage level.

13. A multi-chip package device comprising:

a plurality of package terminals;

a semiconductor memory chip having a test circuit, a plurality of address input terminals, a high voltage input terminal and a test terminal, the test circuit is enabled when a high voltage level is applied to the test terminal; and

an interface chip connected to the package terminals and the semiconductor memory, the interface chip including,

a control circuit having a plurality of memory terminals connected to the package terminals and a plurality of address terminals for providing address signals based on signals received from the memory terminals, the control circuit generating a test signal and an enable signal in response to the received signals,

a high voltage generating circuit connected to the control circuit, the high voltage generating circuit generates a high voltage signal having the high voltage level in response to the enable signal, and

a transferring circuit connected to the

control circuit, the high voltage circuit and the high voltage input terminal and the test terminal of the memory chip, the transferring circuit providing the high voltage signal to the memory chip in response to the test signal.

14. A multi-chip package device according to claim 13, wherein the memory terminals are serial interface memory terminals.

15. A multi-chip package device according to claim 14, wherein the serial interface memory terminals includes a chip select terminals, a serial data input terminal, a serial data output terminal and a clock input terminal.

16. A multi-chip package device according to claim 13, wherein the memory chip is a general purpose memory chip.

17. A multi-chip package device according to claim 13, wherein the transferring circuit includes a P channel MOS transistor having a gate connected to receive the test signal, a first terminal connected to receive the high voltage signal and a second terminal connected to the test terminal.

18. A multi-chip package device according to claim 13, wherein the control circuit receives the high voltage signal, and wherein the test signal has the high voltage level.